Implementation of Hilbert transformation in FPGA

Team Name: **Casper**

Khagesh Patel

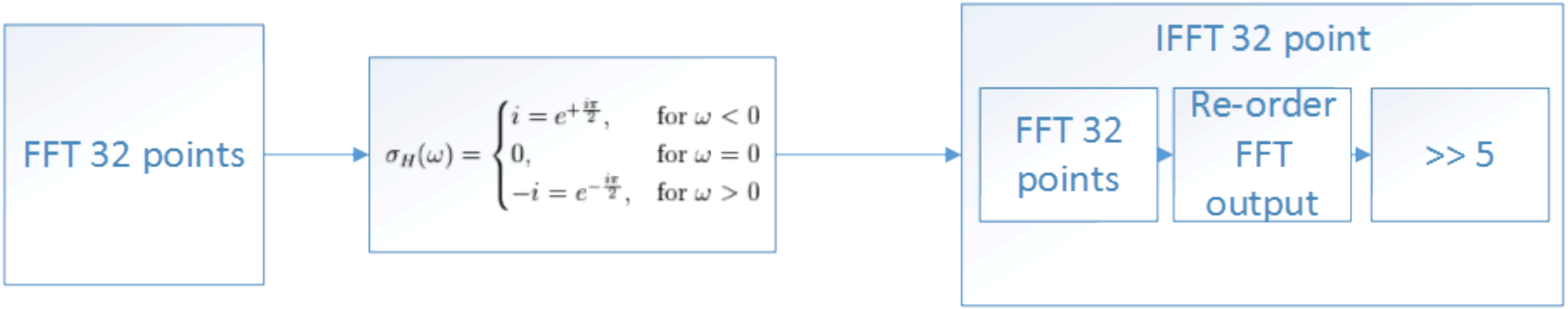
Chaitanya Ahuja

Basics (Bit Representation)

- 32-bit representation with 16-bit floating

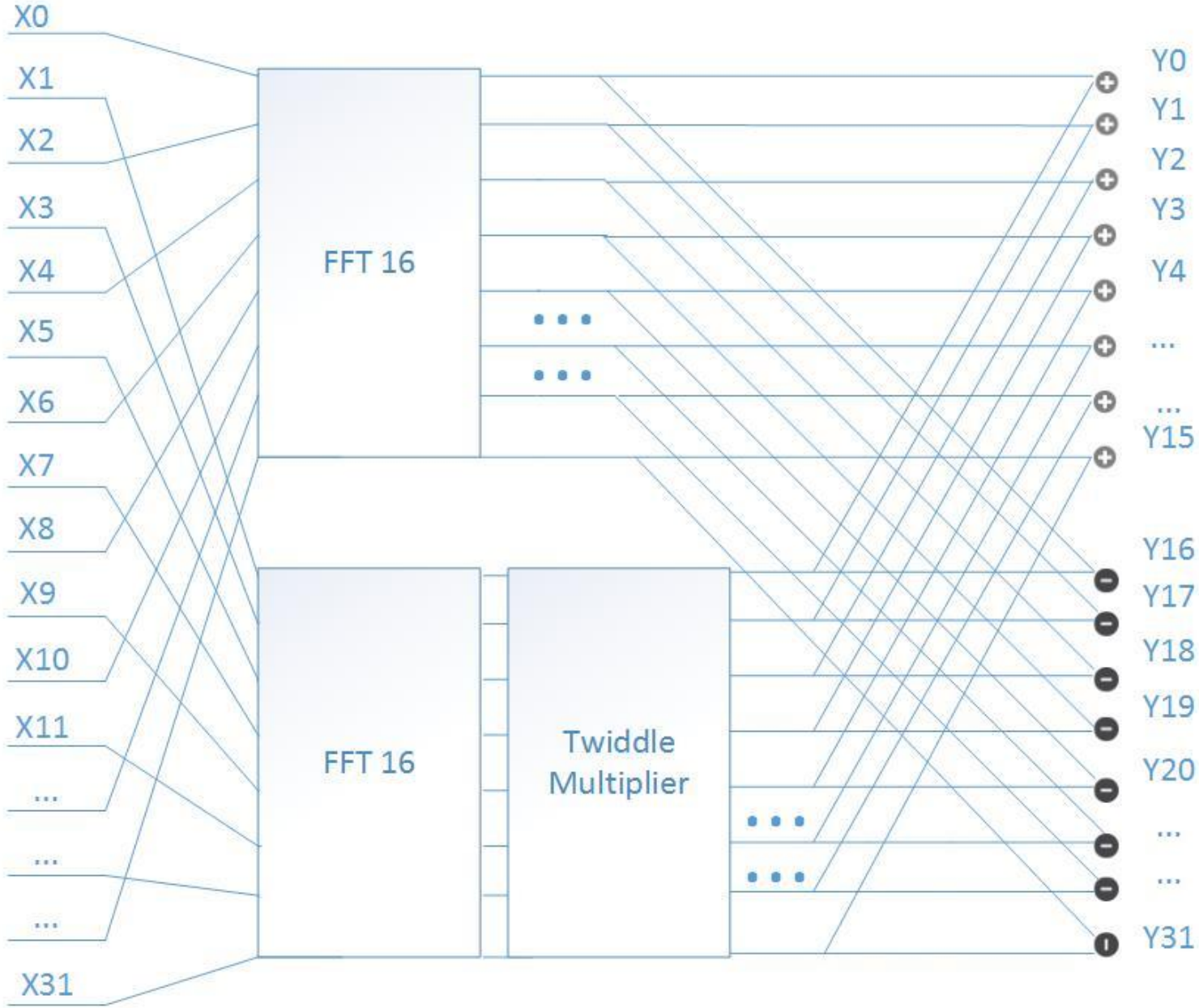
- Avoided floating in hardware,
  - All the calculations are performed on numbers already multiplied by 2^{16}

Algorithm for Hilbert Transform

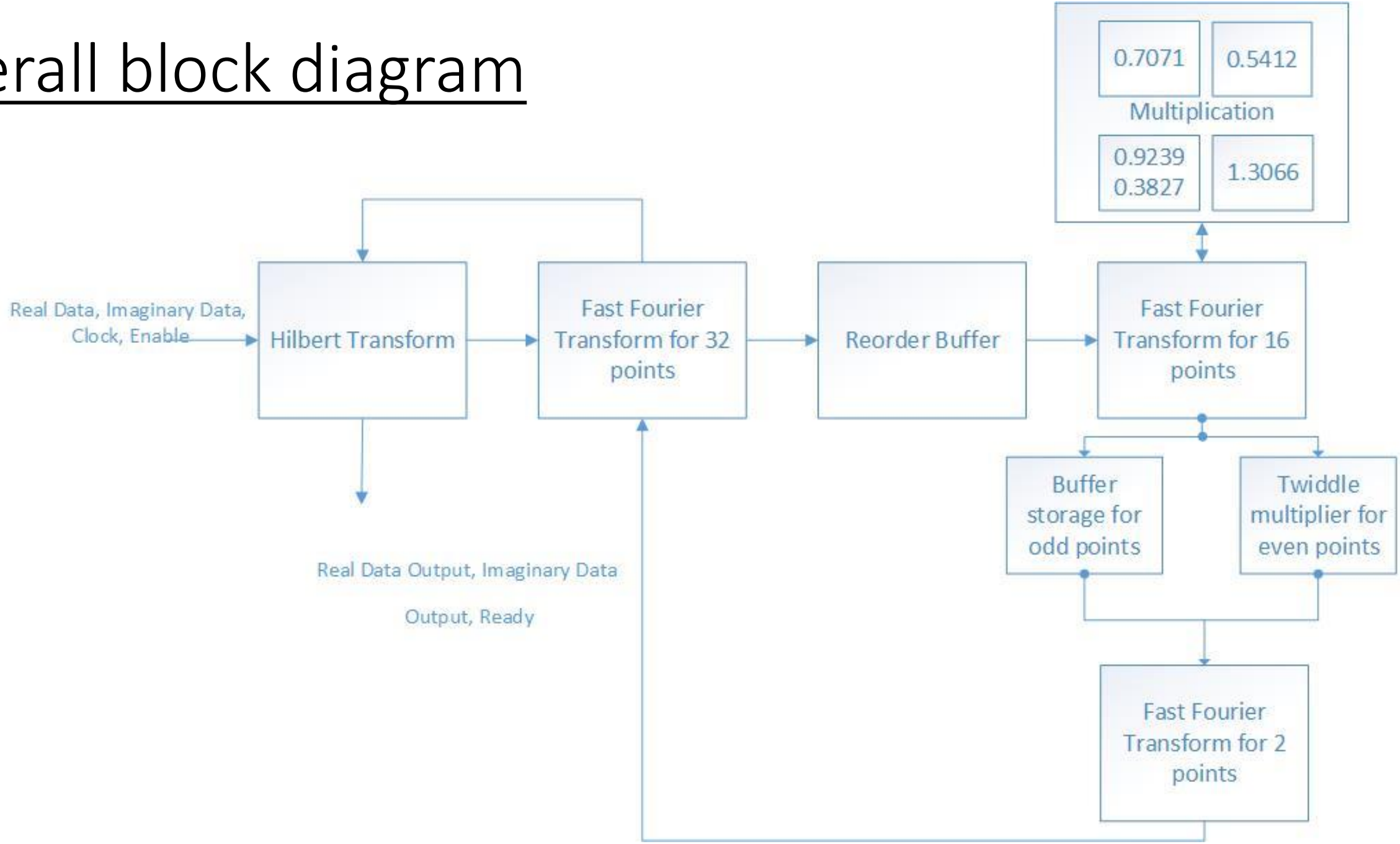


$$\mathcal{F}^{-1}(\{x_n\}) = \mathcal{F}(\{x_{N-n}\})/N$$

FFT 32 Motivation



Overall block diagram



FFT 32 Implementation

- Is implemented using **FFT 16** and **FFT 2** blocks.
- **Pipelined approach** instead of fully parallel architecture.
  - **Less hardware** requirement.
  - **More clock** cycles **(Optimized)**
- One pass through FFT32 requires **96 clock cycles**.
- **Twiddle multiplier** constants can be **stored in external memory** thereby **reducing hardware requirement** further.

16 point FFT implementation

- Implemented using Rader's Algorithm given in ***Fast Fourier Transform and Convolution Algorithms by "H. J. Nussbaumer".***

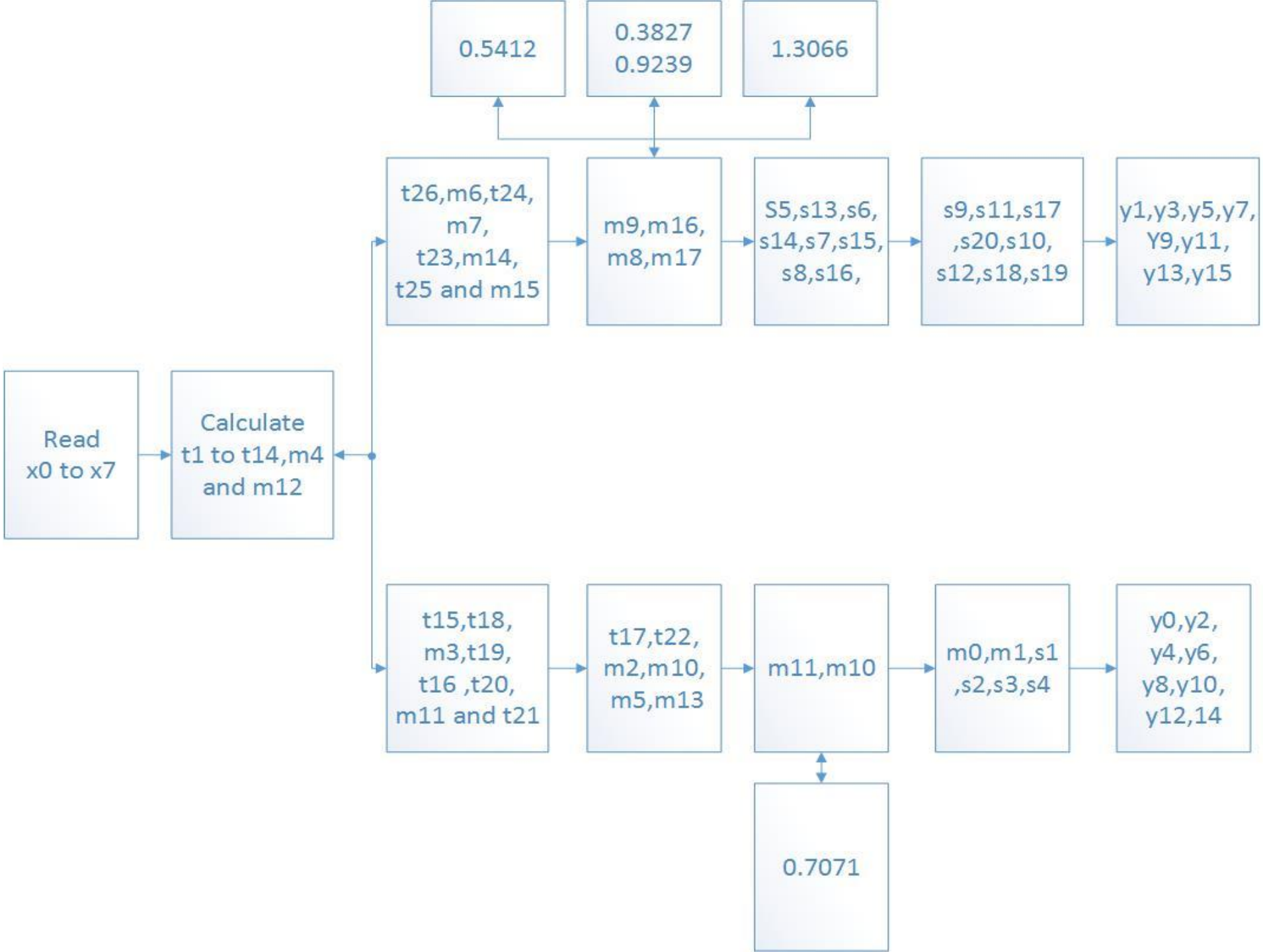
  - *Refer to PDF **for RADER's Algorithm***

- Requires approximately **30 clock cycles** to return first output.

- **Even and odd outputs are running in parallel** for most of the operation as calculations due to even and odd data points are independent.

- **Even and Odd** evaluations in themselves are **pipelined** to achieve the optimal memory time balance.

- Only **Four** Specialized **multiplication units** are used.



Pipelined diagram for FFT 16.

Advantages

Method	Multiplications	Additions	Twiddle factors in LUT
Simple 16pt FFT using Basic 2pt Butterfly	24	64	14
Rader's Algorithm	18	74	5

- **Lesser number of multiplication** leads to **decrease in truncation error** and **hardware consumption**.
- **Lesser number of twiddle factors** means **lesser memory requirement**, **lesser hardware requirement** and **lesser chances of error propagation**.

Multiplication Factors

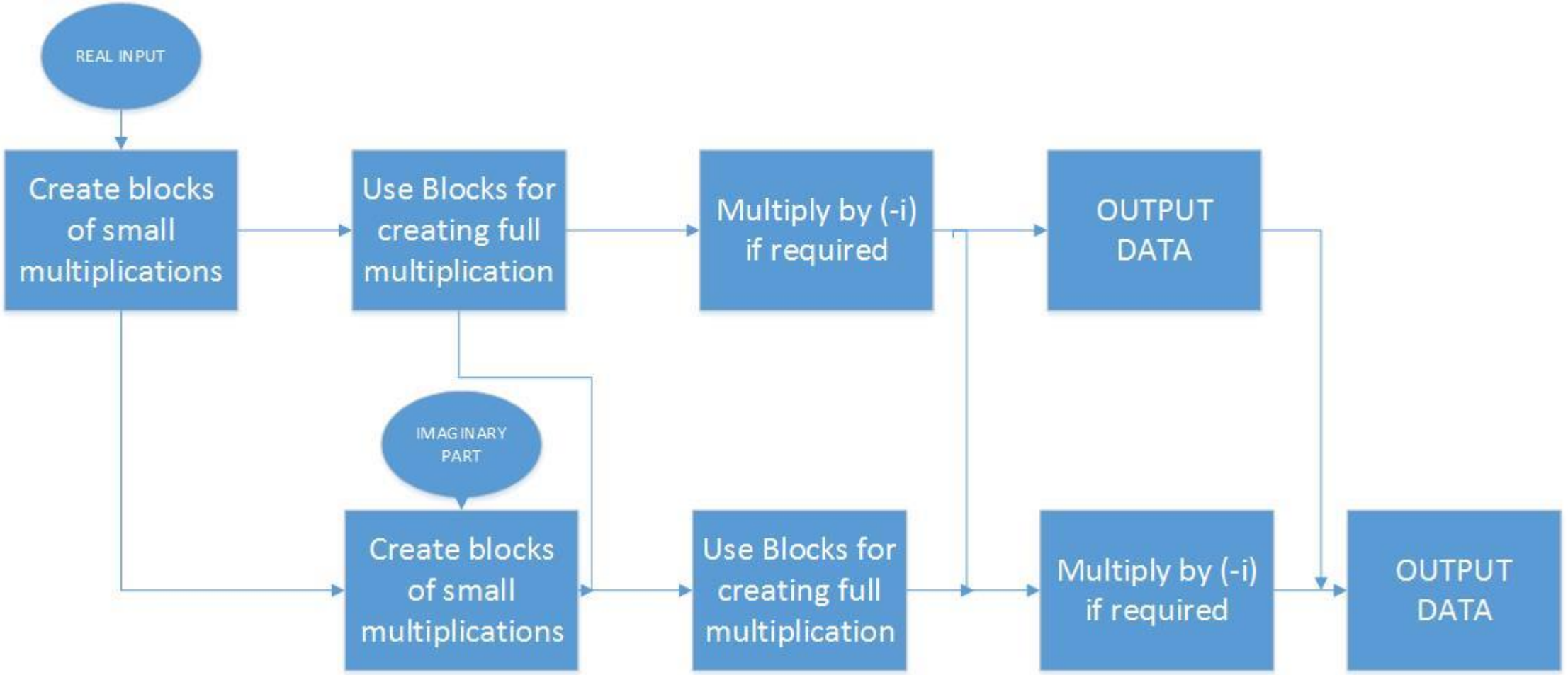
- $\cos\left(\frac{\pi}{4}\right)$=0.7071=0.1011010100000100
- $\cos\left(\frac{3\pi}{8}\right) = 0.3827$=0.0110000111111000
- $\cos\left(\frac{\pi}{8}\right) = 0.9239$=0.1110110010000100
- $\cos\left(\frac{\pi}{8}\right) + \cos\left(\frac{3\pi}{8}\right)$=1.3066=1.0100111001111110
- $\cos\left(\frac{\pi}{8}\right) - \cos\left(\frac{3\pi}{8}\right)$=0.5412=0.1000101010001100

Multiplication

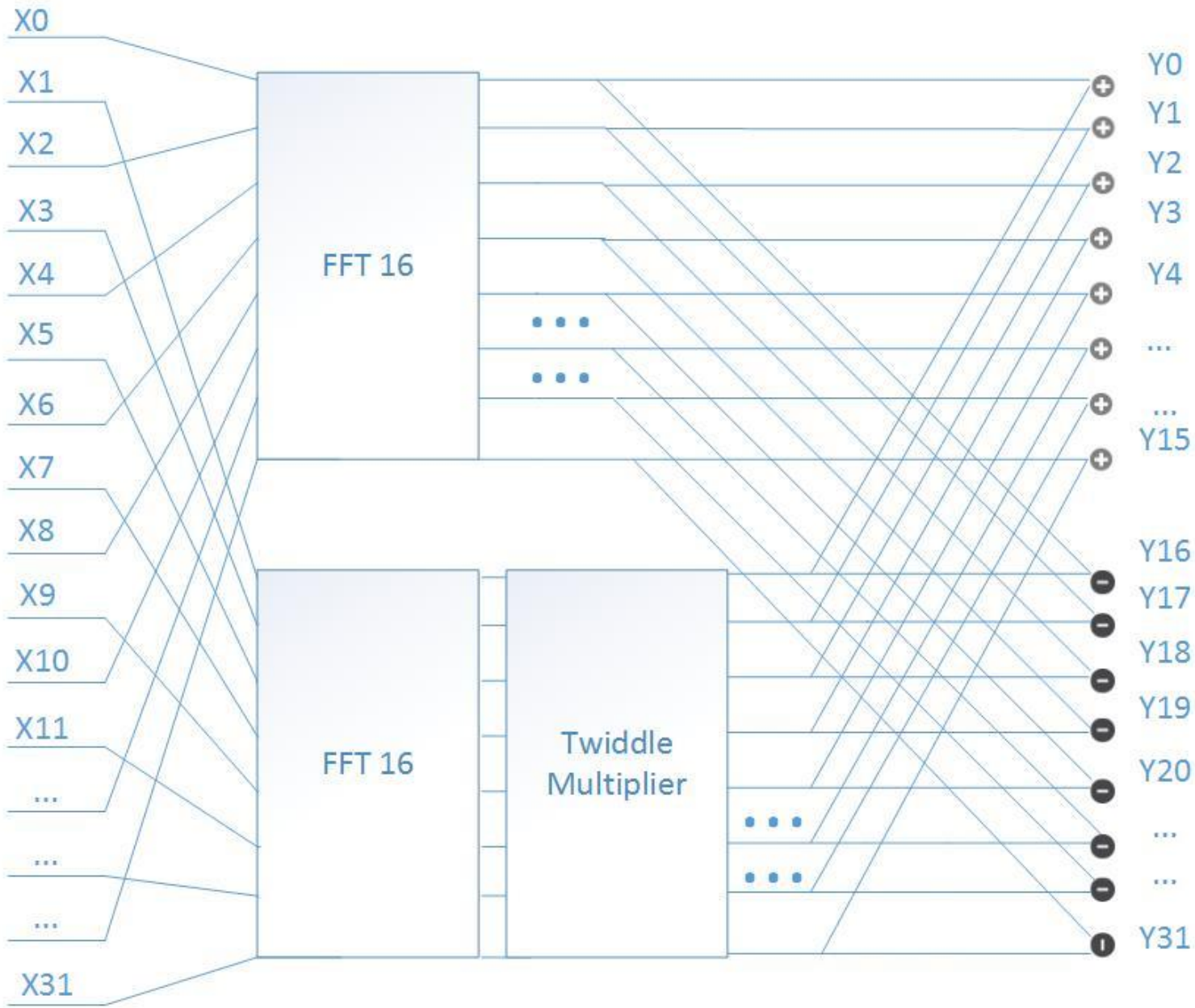
- Multiplication of REAL and IMAGINARY **pipelined** to save memory.
- **Small Blocks** of calculations (for eg. Multiplication with 5 or 3) is performed.
- These **small blocks are combined** to get complete multiplication

- For eg. Lets take Multiplication with $(0.5412)_{10} * 2^{16} = (1000\ 1010\ 1000\ 1100)_2$
- Clearly, $(101)_2$=(5) and $(11)_2$=(3), hence we can use these small blocks for full calculations.
- **Final output** of this multiplication is a **32-bit number**.

Multiplication Module (Block Diagram)

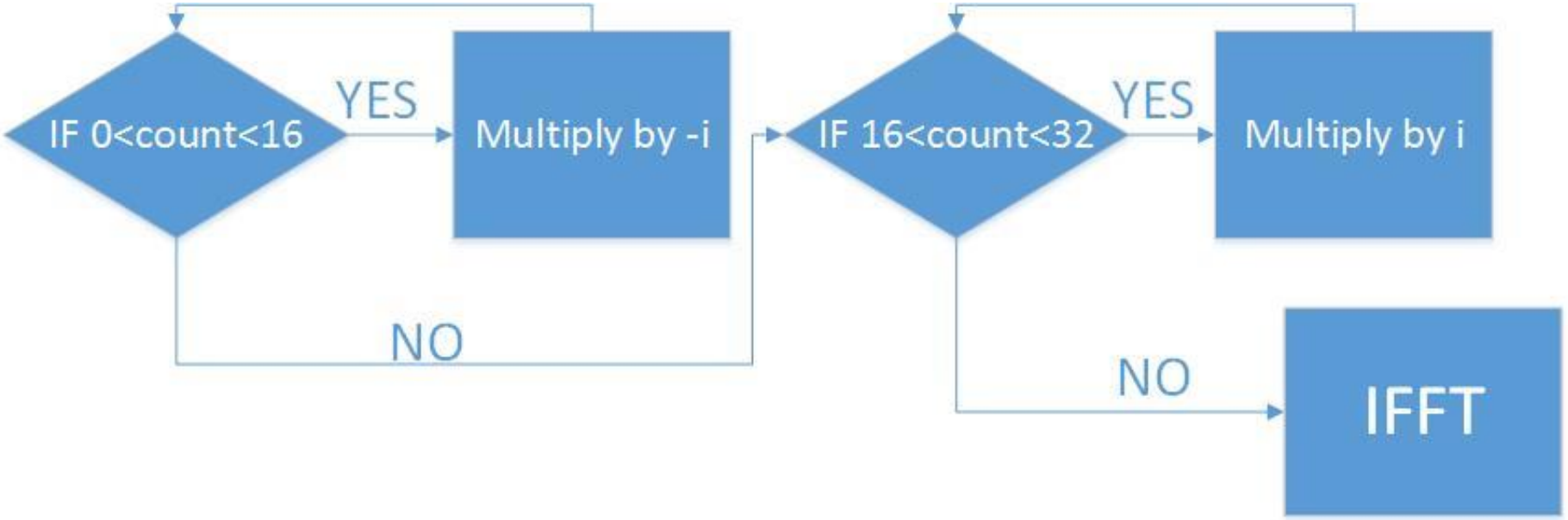


FFT 32


X0
X1
X2
X3
X4
X5
X6
X7
X8
X9
X10
X11
...
...
...
X31
FFT 16
FFT 16
Twiddle Multiplier
Y0
Y1
Y2
Y3
Y4
...
...
Y15
Y16
Y17
Y18
Y19
Y20
...
...
Y31

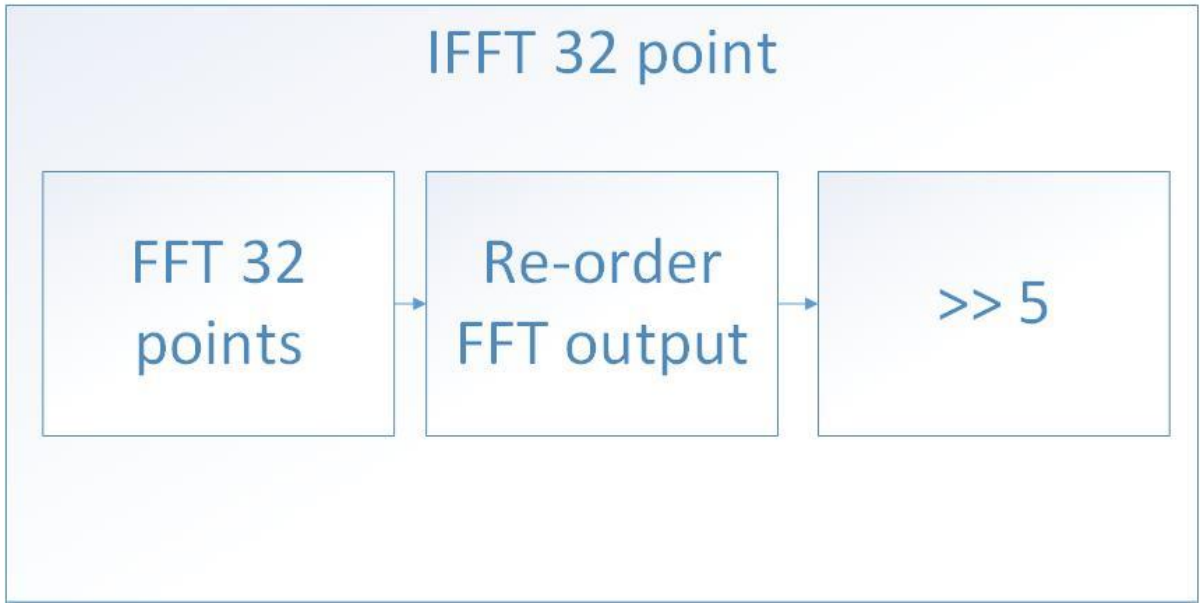
Hilbert Transform

- Usage of FFT of $\frac{1}{\pi n}$ which is $f(n) = \begin{cases} 0, & n = 0 \; or \; n = N/2 \\ -i, & \frac{N}{2} - 1 \geq n \geq 1 \\ i, & \frac{N}{2} + 1 \geq n \geq N - 1 \end{cases}$



IFFT

- Computation based on $\mathcal{F}^{-1}(\{x_n\}) = \mathcal{F}(\{x_{N-n}\})/N$
- **Same** FFT Block used for computation of FFT.
- **Simple Rearrangement** operations and **“divide by 32”** operation yields IFFT.

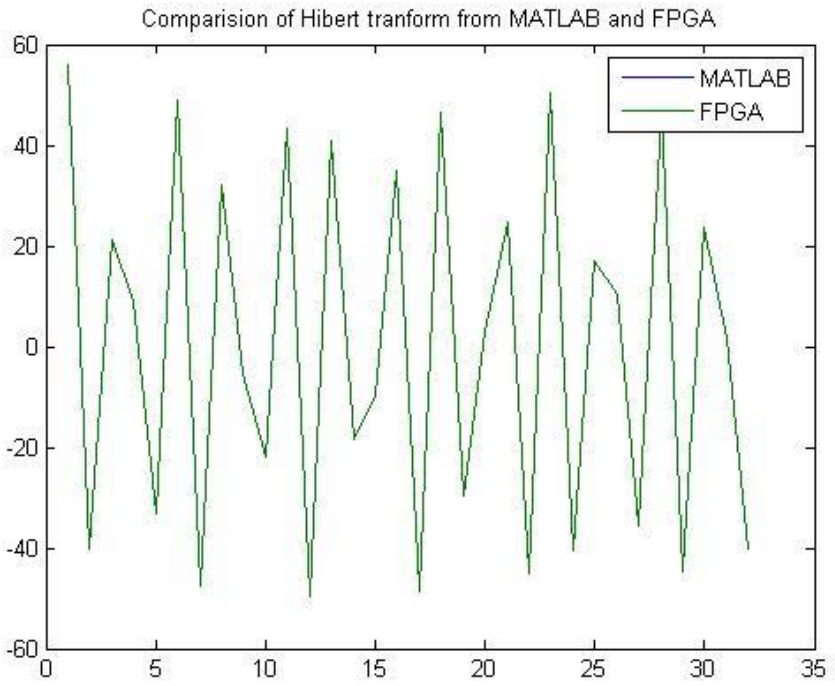


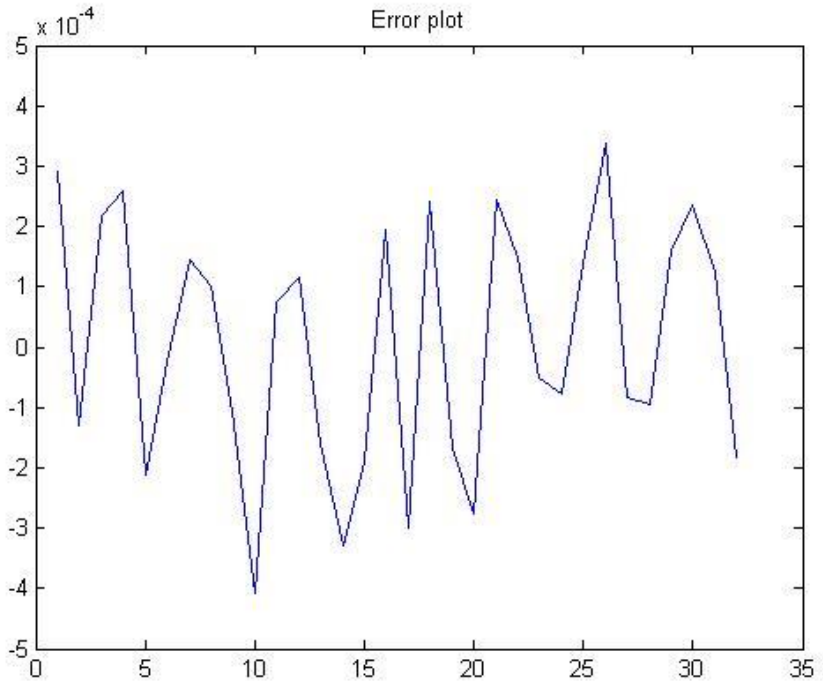
Summary of Innovations

- Use of **Optimized Algorithm** for FFT 16 – with reduced number of **multiplications and twiddle factor** storage
- Used **precision multiplication blocks (Number=4)** for calculations of intermediate steps of FFT 16 algorithm.
- **Same hardware** used for calculation of **first stage of IFFT.**

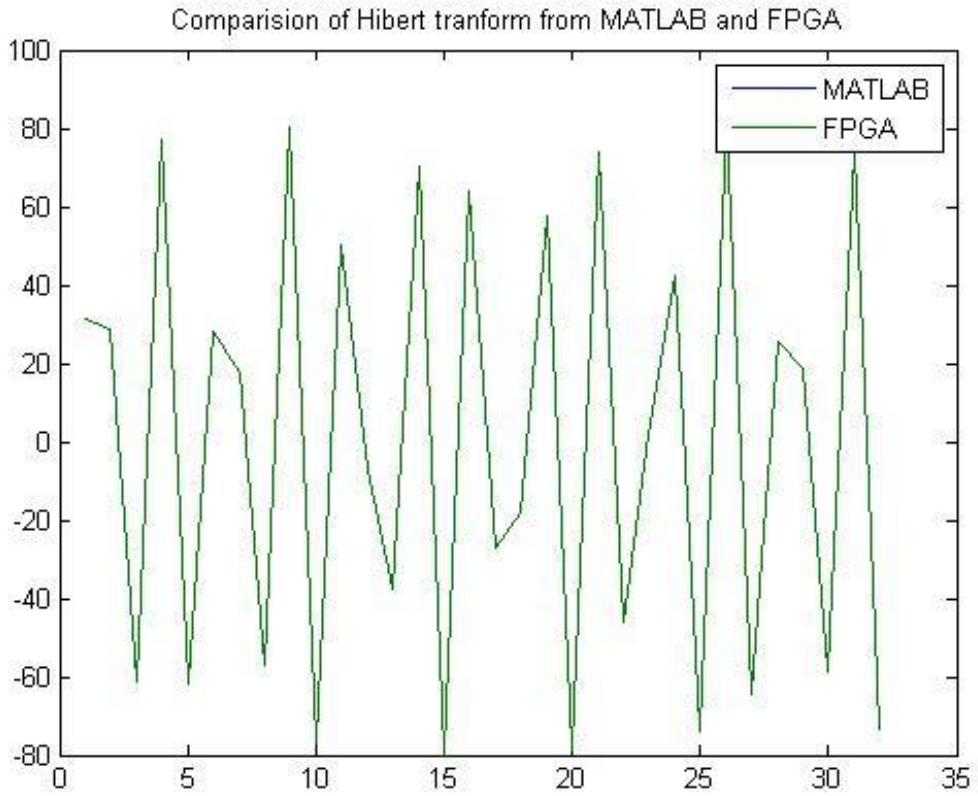
Result for test cases

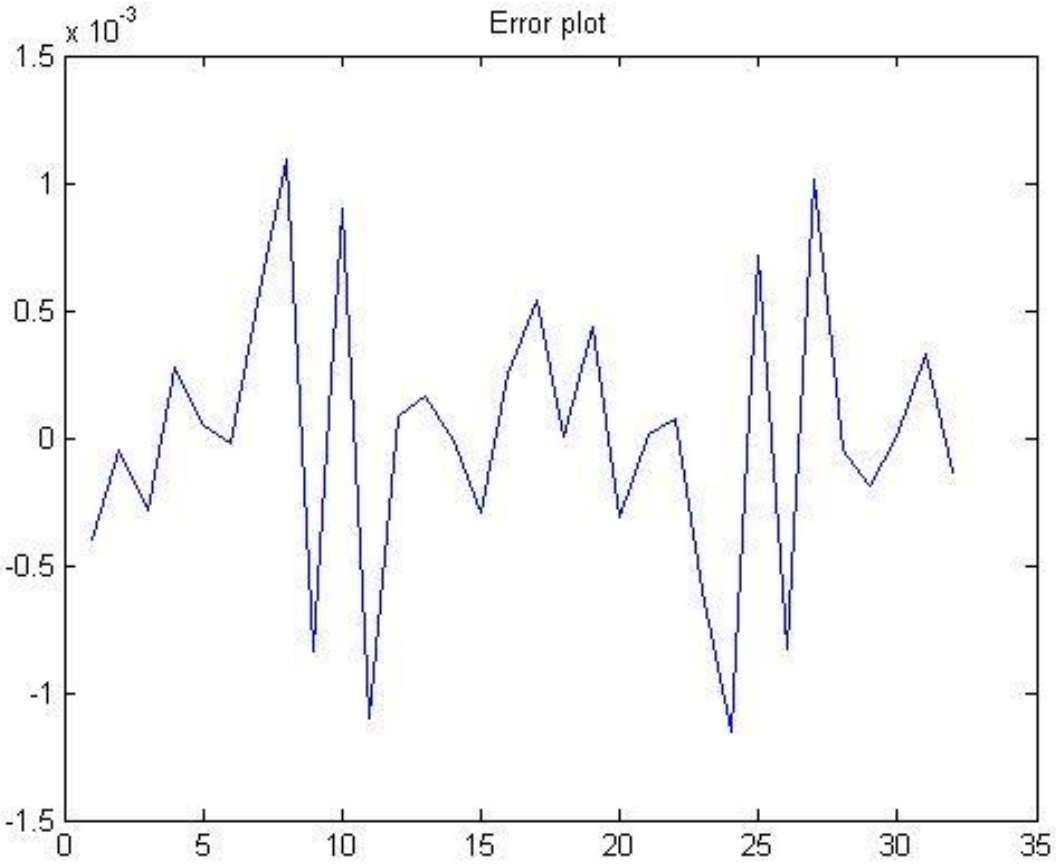
Input wave form	Maximum absolute error	Least square error
50 sin(100t)	$4.0842*10^{-4}$	$1.3158*10^{-6}$
10 sin (100t)+ 80 cos (100t)	0.0011	$9.4172*10^{-6}$





Plots for 50 sin(100t)





Plots for 10 sin (100t)+ 80 cos (100t)

Hardware consumption

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	7106	2443200	0%
Number of Slice LUTs	10380	1221600	0%
Number of fully used LUT-FF pairs	5264	12222	43%
Number of bonded IOBs	133	1200	11%
Number of Block RAM/FIFO	1	1292	0%
Number of BUFG/BUFGCTRLs	1	128	0%
Number of DSP48E1s	16	2160	0%

- Total number of clock cycles: 276 .

References

- *Fast Fourier Transform and Convolution Algorithms by* "H. J. Nussbaumer".

- *Discrete Time Signal Processing by* "Alan V. Oppenheim, Ronald W. Schafer"